REMARKS

This is in response to the Office Action dated March 25, 2003. Non-elected claims 19 and 21 have been canceled, without prejudice in view of the Restriction Requirement. New claims 22-27 have been added. Thus, claims 1-12, 18, 20 and 22-27 are now pending. Attached hereto is a marked-up version of the changes made to the claim(s) by the current amendment. The attached page(s) is captioned "Version With Markings To Show Changes Made." All arguments previously made by applicant in connection with this case are no longer relied upon and are hereby expressly withdrawn.

General

For purposes of example and without limitation, certain example embodiments of this invention relate to a transistor for use in a semiconductor device. A first example embodiment of the instant invention is illustrated with respect to Figures 1-4 of the application, and includes semiconductor substrate 1, first gate electrode 4 provided on the substrate with intervention of gate insulator 2, second electrode 8, and a pair of spaced apart impurity regions. As shown in Figure 4, each of the impurity regions includes a low concentration impurity region 5, an intermediate concentration impurity region 9, and a high concentration impurity region 10 (source/drain). As illustrated, the low, intermediate, and high concentration impurity regions 5, 9 and 10, respectively, are sequentially arranged in this order from a region located under electrode 4 and/or 8 so that the high concentration impurity region 10 is laterally offset from and spaced apart from the low concentration impurity region 5. This arrangement of low, intermediate, and high concentration impurity regions enables the semiconductor device to have a

higher breakdown voltage thereby providing for improved performance and/or reliability (e.g., page 23, lines 8-21). Moreover, the high concentration impurity region 10 is not in contact with a portion of the substrate in which no impurity region is formed; this enables a high breakdown voltage to be achieved.

Furthermore, the second electrode 8 extends beyond a peripheral edge of the first gate electrode 4 so that the second electrode 8 overlaps both the first electrode 4 and at least part of the impurity region(s) 5, 9 and/or 10. With this construction, resistance to pressure of source/drain regions (a pair of the high concentration impurity regions) can be suitably adjusted by changing the overlapping width of the second electrode and the semiconductor substrate 1. In other words, a semiconductor device having more flexibility in design can be provided (e.g., pg. 23, line 27 to pg. 24, line 9).

Claim 1

Claim 1 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Su. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "at least a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order *from a region located underneath at least one of the first and second electrodes*; wherein *the second electrode extends laterally beyond an edge of the first electrode so that the second electrode is provided over both the first electrode and at least part of at*

least one of the impurity regions with intervention of the intermediate insulating film . . . ." For example, Fig. 4 of the instant application illustrates that the *second electrode 8 extends laterally beyond an edge of the first electrode 4* so that the second electrode 8 is provided over both the first electrode 4 and at least part of at least one of the impurity regions with intervention of the intermediate insulating film 6. As explained above, an example advantage associated with this construction is that resistance to pressure of source/drain regions (a pair of the high concentration impurity regions) can be suitably adjusted by changing the overlapping width of the second electrode and the semiconductor substrate 1. Fig. 4 also illustrates that low, intermediate and high concentration impurity regions 5, 9 and 10, respectively, are arranged in this order *from a position under electrode(s) 4 and/or 8*, and wherein the high concentration impurity region 10 is laterally offset from and laterally spaced from the low concentration impurity region 5. Su fails to disclose or suggest the aforesaid underlined aspects of claim 1.

Su cannot anticipate amended claim 1 for at least the two different reasons (1) and (2) set forth below.

(1) Su discloses floating gate electrode 7b, control gate electrode 10, and impurity regions 17, 20 and 23. However, Su is significantly different from the invention of claim 1 since Su's floating and control gate electrodes 7b and 10 are of the *same size*. In other words, Su's control gate electrode 10 does not extend "laterally beyond an edge of the" floating gate 7b, and Su's control gate electrode 10 is not provided over both the floating gate 7b and at least part of at least one of the impurity regions with intervention of the intermediate insulating film. Su is entirely unrelated to the invention of claim 1 in these

respects. Accordingly, Su cannot realize the example advantage associated with this structure (changing the overlapping width of the second electrode and the semiconductor substrate 1 so that resistance to pressure of source/drain regions can be suitably adjusted).

(2) Additionally, since Su's control gate electrode 10 does not extend laterally beyond an edge of the floating gate 7b, the reference also fails to disclose or suggest the requirement of claim 1 of "a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order *from a region located underneath at least one of the first and second electrodes.*" The Office Action contends that region 17 is a low concentration region, while region 20 is an intermediate concentration region and region 23 is of high concentration. However, regions 17, 20 and 23 in Su are not "sequentially arranged in this order *from a region located underneath at least one of the first and second electrodes*" as required by claim 1. In particular, regions 17, 20 and 23 in Su cannot be lined up in this order from any point located "underneath" electrode(s) 7b and/or 10. Again, Su fails to disclose or suggest this aspect of claim 1 as well.

Claim 20

Claim 20 requires "at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes along a horizontal direction of the semiconductor substrate; and wherein the second electrode extends laterally beyond an edge of the first electrode so that the second electrode is provided over both the first

electrode and at least part of at least one of the impurity regions with intervention of at least the intermediate insulating film."

Su fails to disclose or suggest both of the aforesaid underlined aspects of claim 20. In particular, Su's control gate electrode 10 does not extend "laterally beyond an edge of the" floating gate 7b, and Su's control gate electrode 10 is not provided over both the floating gate 7b and at least part of at least one of the impurity regions with intervention of the intermediate insulating film. Additionally, regions 17, 20 and 23 in Su are not "sequentially arranged in this order from a region located underneath at least one of the first and second electrodes along a horizontal direction of the semiconductor substrate" as required by claim 20. For both of these reasons, claim 20 clearly defines over Su.

Claim 22

Claim 22 requires that "the second electrode extends laterally beyond an edge of the first electrode so that the second electrode overlaps each of the first electrode and at least part of said low concentration impurity region and said intermediate concentration impurity region of at least one of said impurity regions of the second conductivity type." For example, see Fig. 4 of the instant application where second electrode 8 extends laterally beyond an edge of first electrode 4 so that the second electrode 8 overlaps each of the first electrode 4 and at least part of low concentration impurity region 5 and intermediate concentration impurity region 9.

Again, the cited art fails to disclose or suggest this aspect of claim 22.

Claim 23

Claim 23 requires that "a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes; wherein an overlapping width of the first electrode and a first one of said pair of impurity regions of the second conductivity type is *different* than an overlapping width of the first electrode and a second one of said pair of impurity regions of the second conductivity type." For example, see Exhibit 1 attached hereto which includes a marked-up version of Fig. 9 of the instant application for the Examiner's convenience. It can be seen in Fig. 9 of Exhibit 1 attached hereto that an overlapping width of the first electrode 4 and a first one of said pair of impurity regions of the second conductivity type is *different* than an overlapping width of the first electrode 4 and a second one of said pair of impurity regions of the second conductivity type. In other words, in Exhibit 1, $A \neq B$.

The cited art fails to disclose or suggest this aspect of claim 23. For example, Su's electrode 7b overlaps the impurity regions on either side thereof to the same extent, thereby teaching directly away from the invention of claim 23.

Additionally, regions 17, 20 and 23 in Su are not "sequentially arranged in this order from a region located underneath at least one of the first and second electrodes" as required by claim 23. In Su, regions 17, 20 and 23 in Su cannot be lined up in this order from any point located "underneath" electrode(s) 7b and/or 10.

Su fails to disclose or suggest each of the aforesaid two aspects of claim 23.

Claims 24 & 25

Claims 24 and 25 require that "a distance from (a) an edge of the high concentration impurity region closest to the first electrode to (b) an edge of the intermediate concentration impurity region closest to the first electrode in a first one of said pair of impurity regions of the second conductivity type is different from the corresponding distance from (a) to (b) in a second of said pair of impurity regions of the second conductivity type." For example, see Exhibit 1 attached hereto which includes a marked-up version of Fig. 6 of the instant application for the Examiner's convenience. In particular, in Exhibit 1, $X \neq Y$ in marked-up Fig. 6.

Su is entirely unrelated to the inventions of claims 24 and 25. In particular, Su teaches directly away from these claims because Su's diffusion regions on either side of the gate electrodes are symmetrical.

Claim 26

Claim 26 requires "the second electrode extends laterally beyond an edge of the first electrode so that the second electrode is provided over both the first electrode and at least part of at least one of the impurity regions with intervention of the intermediate insulating film." Again, Su fails to disclose or suggest this aspect of claim 26 since Su's electrodes 7b and 10 are the same size.

Claim 27

Claim 27 requires "***the entirety of*** the high concentration impurity region is laterally offset from and laterally spaced from the low concentration impurity region in said one impurity region." For example, Fig. 4 of the instant application illustrates that ***the entirety of*** the high concentration impurity region 10 is laterally offset from and

laterally spaced from the low concentration impurity region 5 in at least one impurity region.

Su clearly fails to disclose or suggest this aspect of claim 27. In Su the "entirety" of high concentration impurity region 23 is not laterally offset from the alleged low concentration impurity region 17. Instead, high concentration region 23 is directly below a central portion of region 17, thereby teaching directly away from the invention of claim 27.

Conclusion

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE CLAIMS

1. (Amended) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film;

at least a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes;

wherein the second electrode extends laterally beyond an edge of the first electrode so that the second electrode is provided over both the first electrode and at least part of at least one of the impurity regions with intervention of the intermediate insulating film; and

wherein the high concentration impurity region is laterally offset from and laterally spaced from the low concentration impurity region in said at least one impurity region.

20. (Amended) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film;

a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes along a horizontal direction of the semiconductor substrate; and

wherein the second electrode extends laterally beyond an edge of the first electrode so that the second electrode is provided over both the first electrode and at least part of at least one of the impurity regions with intervention of at least the intermediate insulating film.

Please add the following new claims:

22. (New) The semiconductor device of claim 1, wherein the second electrode extends laterally beyond an edge of the first electrode so that the second electrode overlaps each of the first electrode and at least part of said low concentration impurity

region and said intermediate concentration impurity region of at least one of said impurity regions of the second conductivity type.

23. (New) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film;

a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order from a region located underneath at least one of the first and second electrodes;

wherein an overlapping width of the first electrode and a first one of said pair of impurity regions of the second conductivity type is different than an overlapping width of the first electrode and a second one of said pair of impurity regions of the second conductivity type; and

wherein the high concentration impurity region is laterally offset from and laterally spaced from the low concentration impurity region in said at least one impurity region.

24. (New) The semiconductor device of claim 1, wherein a distance from (a) an edge of the high concentration impurity region closest to the first electrode to (b) an edge of the intermediate concentration impurity region closest to the first electrode in a first one of said pair of impurity regions of the second conductivity type is different from the corresponding distance from (a) to (b) in a second of said pair of impurity regions of the second conductivity type.

25. (New) The semiconductor device of claim 20, wherein a distance from (a) an edge of the high concentration impurity region closest to the first electrode to (b) an edge of the intermediate concentration impurity region closest to the first electrode in a first one of said pair of impurity regions of the second conductivity type is different from the corresponding distance from (a) to (b) in a second of said pair of impurity regions of the second conductivity type.

26. (New) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film;

at least a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions

comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in this order;

wherein the second electrode extends laterally beyond an edge of the first electrode so that the second electrode is provided over both the first electrode and at least part of at least one of the impurity regions with intervention of the intermediate insulating film; and

wherein the high concentration impurity region is spaced apart from the low concentration impurity region in said at least one impurity region.

27. (New) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

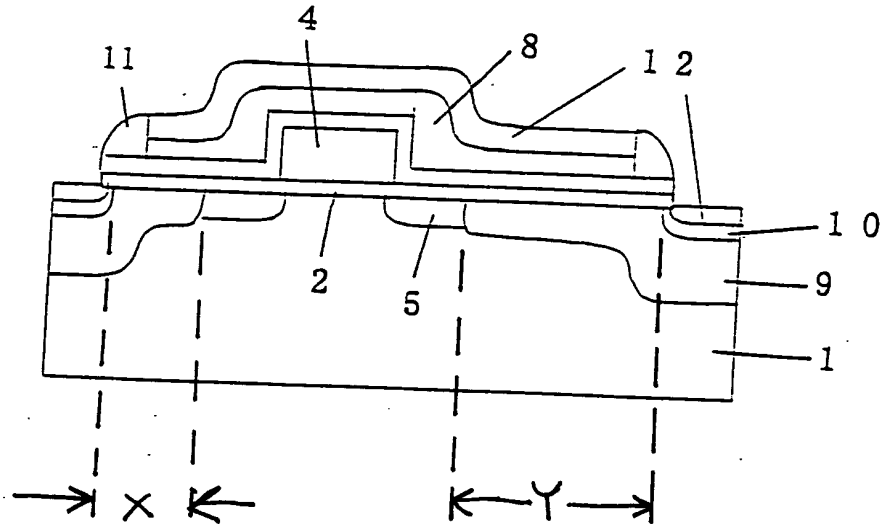
a first electrode provided on the semiconductor substrate with the intervention of a gate insulation film;

a second electrode provided at least on the first electrode with the intervention of an intermediate insulation film;

at least a pair of impurity regions of a second conductivity type provided in a spaced relation in the semiconductor substrate, at least one of the impurity regions comprising a low concentration impurity region, an intermediate concentration impurity region and a high concentration impurity region sequentially arranged in said one impurity region in this order from a region located underneath at least one of the first and second electrodes; and

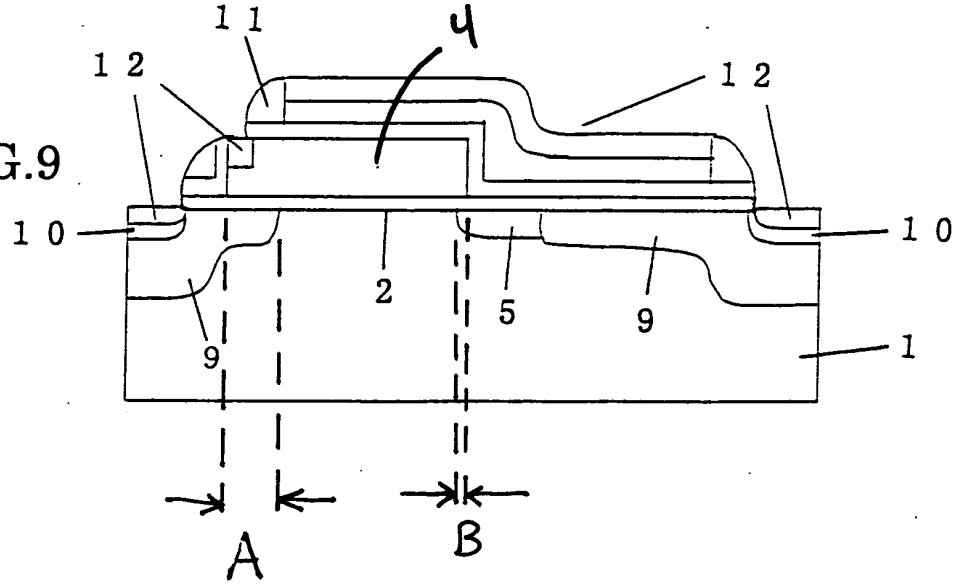
wherein the entirety of the high concentration impurity region is laterally offset from and laterally spaced from the low concentration impurity region in said one impurity region so that the high and low concentration impurity regions are each provided in the same impurity region.

FIG.6



$X \neq Y$

FIG.9



$A > B$

Exhibit 1 → Marked-up Figs. 6+9 for Examiner's Convenience